Implementation of Amplitude Modulation on Software Defined Radio

K.Satyanarayana[1], Madhekar Suneel[2], Ravi Ranjan[2]
[1]Indian Institute of Technology-Madras, Chennai-600036, ee10b014@ee.iitm.ac.in
[2]PGAD, Defence Research and Development Organisation, Hyderabad-500058, cybersuneel@gmail.com and raviranjan222@gmail.com

***Abstract*—An amplitude modulation transceiver design is presented, using a software defined radio platform. Model based design is used to implement the various transmitter and receiver blocks. The wireless communication of audio signals is demonstrated.**

***Index Terms*—Software radio, wireless communication, amplitude modulation, demodulation.**

I. Introduction

This papers presents a design of an amplitude modulation (AM) transceiver. The modulation scheme used is double sideband modulation. The demodulation is carried out using an envelope detector. The entire implementation is carried out on a software defined radio (SDR) platform. The SDR platform used is the Lyrtech Small Form Factor (SFF) platform. Model based design is used as the design method. This method relies on Matlab®, Simulink®, Texas Instruments® Code Composer Studio® and Xilinx® blocks.

II. Amplitude Modulation

Amplitude modulation is defined as a process in which the amplitude of the carrier wave $A_c\cos(2\pi f_c t)$ is varied about a mean value, linearly with the baseband message signal $m(t)$, where, A_c is the carrier amplitude, f_c is the frequency of the carrier signal and t is time. The amplitude modulated signal is given by

$$s(t) = A_c\left[1 + k_a m\left(t\right)\right]\cos\left(2\pi f_c t\right) , \tag{1}$$

where, k_a is the amplitude sensitivity of the modulation scheme. In frequency domain, this can be expressed as

$$\begin{aligned} S\left(f\right) = \frac{A_c}{2}\left[\delta\left(f - f_c\right) + \delta\left(f + f_c\right)\right] + \\ \frac{k_a A_c}{2}\left[M\left(f - f_c\right) + M\left(f + f_c\right)\right] . \end{aligned} \tag{2}$$

III. Software Defined Radio

SDR is a wireless technology created to improve interoperability between different wireless networks, field radios, and devices. With this technology, we can create multi-mode, multi-band, and multi-functional wireless devices and network equipment that can be dynamically reconfigured, enhanced, and upgraded through software updates and hardware reconfiguration. An SDR consists of three main modules Fig 2, namely, data conversion module, digital signal processing module and RF section module [2]. A picture of the SDR platform used to carry out this work is shown in Fig 1.

Fig. 1: SDR platform with mobile phone as audio source

A. Digital signal processing module

The digital signal processing (DSP) module contains a six core TMS320DM6446DSP processor, and a Xilinx® Virtex-4® FPGA. The processor is clocked at 594 MHz. The processor and the FPGA form the main signal processing devices of the radio platform. The DSP module also contains an audio codec.

B. Data conversion module

This module contains two analog input channels with 14 bit, 125 MSPS analog to digital converters (ADC). The ADC used is a Texas Instruments® ADS5500 [4]. This module also contains two analog outputs driven by a dual channel 16-bit, 500-MSPS digital to analog converter (DAC). The DAC used is a Texas Instruments® DAC5687 [5]. Besides, there are two external clock inputs and on-board clock synthesizer.

C. RF module

This module has a radio frequency transceiver with frequency range 1.6 GHz to 2.2 GHz. The intermediate frequency bandwidth is selectable between 5 MHz and

20 MHz. The maximum gain provided is 22 dB. The RF section sensitivity is -110 dBm at a signal to noise ratio of 10 dB and a signal bandwidth of 1 kHz.

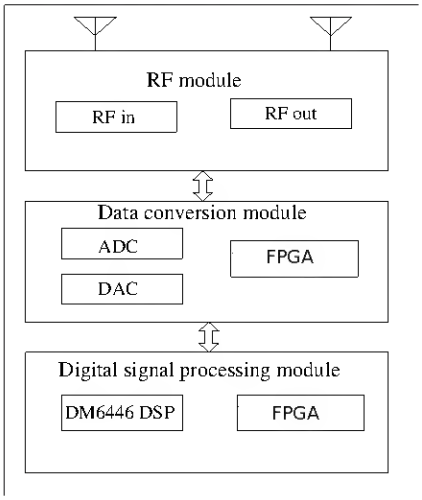

Fig. 2: Schematic of the modules

IV. Description of AM transmitter

The description of the AM transmitter is in two parts, namely, the DSP model and the FPGA model. The DSP model is implemented in the DSP, and acts as an interface between the audio signal source, and the FPGA. With the on-board audio codec as the signal source, a DSP model is shown in Fig 3. The audio codec is configured to

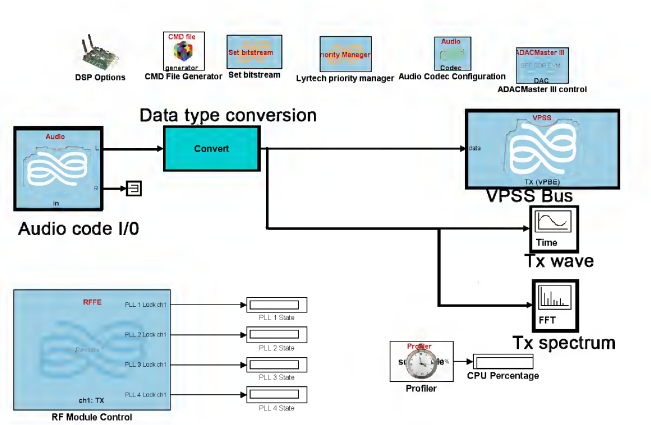

Fig. 3: DSP transmitter model

generate output samples at 24.414 kHz. A Video Processing Subsystem (VPSS) bus is used to communicate the received samples to the FPGA. The VPSS bus provides 32-bit interface between DSP to FPGA and FPGA to DSP. The VPSS bus is provided with the Video Processing Front End (VPFE) directs the signal to DSP and the Video Processing Back End (VPBE) directs the signal to the FPGA. The VPFE is clocked at 75 MHz and the VPBE is clocked at 37.5 MHz. The DSP model also contains blocks to configure the RF section, the audio codec and the ADACMaster-III data conversion module, apart from certain other platform-specific configuration blocks. The FPGA model receives the samples from the DSP, the FPGA model is shown in Fig 4.

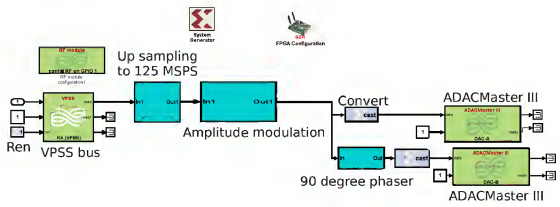

Fig. 4: FPGA model showing AM modulation

The received signal is first upsampled to 125 MSPS, the upsampling to 125 MSPS in Fig 4 is shown in figure 5.

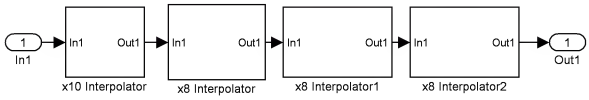

Fig. 5: Upsampling to 125 MSPS

The upsampling by 8 block (x8 interpolator) is implemented as shown in Fig 6. The other upsampling blocks in Fig 5 are implemented in a similar manner.

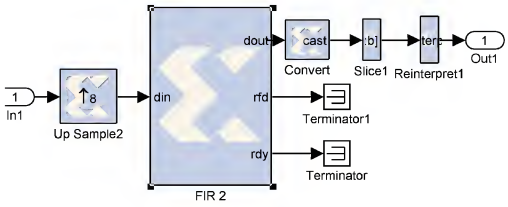

Fig. 6: Upsampling by a factor 8

The upsampled signal is amplitude modulated using a 1 MHz carrier waveform. The carrier is generated using a direct digital synthesis (DDS) block as shown in Fig 7.

The modulated signal is given to the DAC, for upconversion to the Intermediate Frequency (IF). In the DAC, single side band modulation mode is enabled. This IF signal is then given to the RF module for upconversion and transmission. The transmission frequency used in the present work is 1700 MHz.

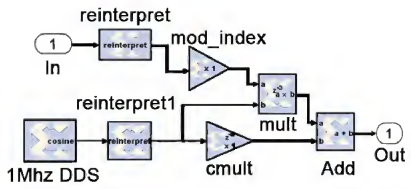

Fig. 7: Amplitude modulation

V. Description of AM receiver

The transmitted signal propagates over the air, and is received by the receive antenna of the RF module. The RF module down-converts it to the IF of 30 MHz. This IF signal is fed to one of the ADC inputs of the ADACMaster-III data conversion module. The digitized signal is provided as input to the signal processing module. In the signal processing module, the description is again in two parts, namely the DSP model and the FPGA model. FPGA model is shown in figure 8.

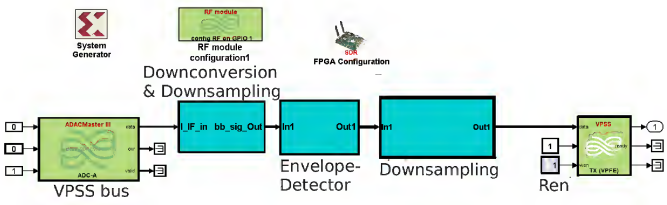

Fig. 8: FPGA model showing AM demodulation

In the FPGA model the signal is first downconverted by 30 MHz , as shown in Fig 9 and downsampled by factor 8 as shown in Fig 10. This down-sampled signal is fed

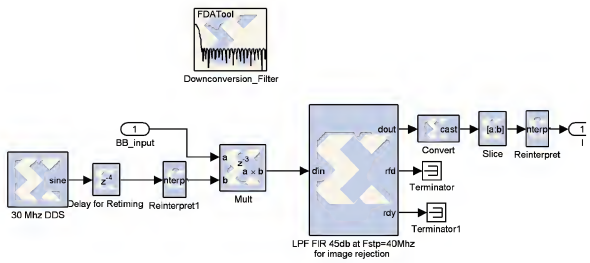

Fig. 9: Downconversion

to the input of an envelope detector block, shown in Fig 11. The envelope detector demodulates the AM signal. The demodulated signal is further down-sampled to 24.414 kHz by downsampling blocks, as shown in Fig 12.

The down-sampling blocks in Fig 12 are implemented in a similar manner as in Fig 10.

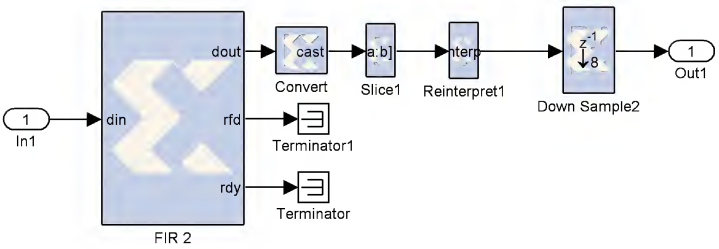

Fig. 10: Downsampling by a factor 8

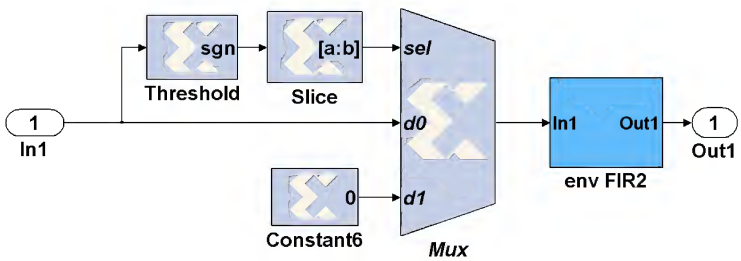

Fig. 11: Envelope Detector

This signal is communicated from the FPGA, using another VPSS bus to the DSP .

In the DSP model this signal is fed to the DC offset block. This block adjusts the DC of the signal. This adjusted signal is fed to the audio codec with samples at 24.414 kHz, as shown in Fig 13.

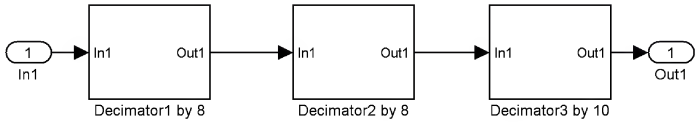

Fig. 12: Downsampling to 24.414 kHz

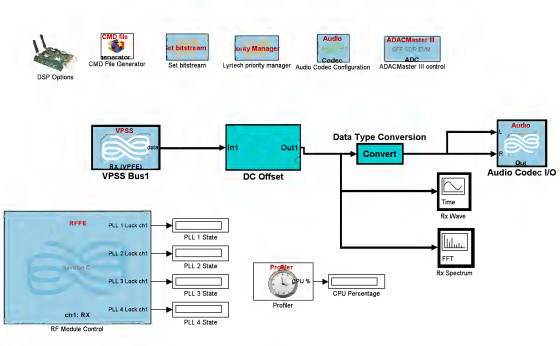

Fig. 13: DSP receiver model

VI. Results

The results are taken from Simulink® so there is a time delay between the transmitted baseband signal and the received signal. There is a DC component in the received spectrum as an effect of envelope detection.

Fig 14 and Fig 15 are baseband signals (audio) from the Tx wave and Tx spectrum in the Fig 3

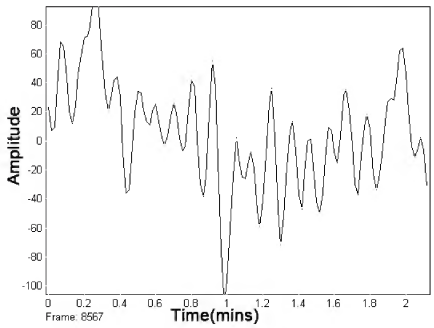

Fig. 14: Signal from audio codec in time domain

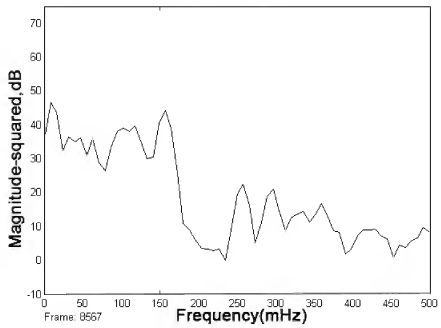

Fig. 15: Signal from audio codec in frequency domain

Fig 16 and Fig 17 are baseband signals (audio) from the Rx wave and Rx spectrum in the Fig 13. The received signal was played back on a speaker and reproduced well.

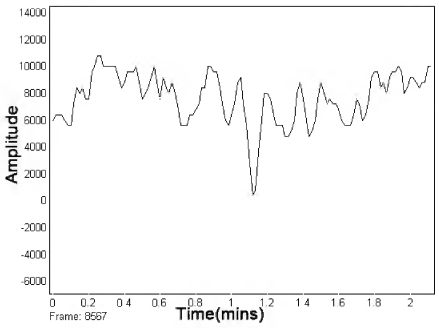

Fig. 16: Received signal in time domain

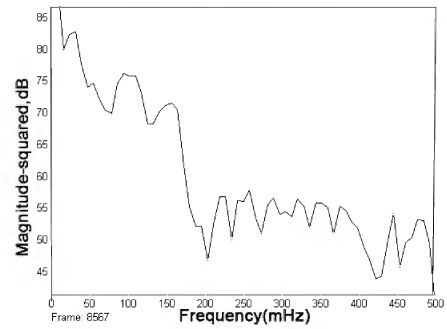

Fig. 17: Received signal in frequency domain

References

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[5] Texas Instruments® DAC5687 datasheet available at http://www.ti.com/lit/ds/symlink/dac5687.pdf